High Performance, Single-Crystal Silicon TFTs for High Resolution Displays

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Abstract

High resolution, emissive micro-displays, such as OLED or MicroLED, demand backplane technology which surpasses current FPD industry standards in both performance and uniformity. Single-crystal Silicon on Glass (SiOG) offers a compelling solution to meet these performance and uniformity requirements. This paper highlights recent breakthroughs in SiOG thin film transistors (TFTs), and the path to achieve sub-micron devices while minimizing leakage current and short-channel effects.

Author Keywords

Single-crystal; TFT; high resolution; emissive display; backplane; SOI; dopant activation; ion implantation.

Objective and Background

High resolution, emissive micro-displays (OLED or MicroLED), demand backplane technology that challenges, in both performance and uniformity, those currently available in the flat panel display (FPD) industry [1]. Single-crystal Silicon on Glass (SiOG) offers the potential to meet these performance and uniformity requirements, with demonstrations of electron and hole effective mobility, μ_{FE} > 450 and 220 cm^2/V s, for micron-scale n-type and p-type devices, respectively [2].

This paper will present the latest advances in SiOG thin film transistors (TFTs), and the path to achieve sub-micron devices while minimizing leakage current and short-channel effects. Single-crystal silicon on display glass substrates is proposed as a competitive technology to low temperature polysilicon (LTPS), amorphous oxide semiconductor (AOS), or low temperature polycrystalline oxide (LTPO).

SiOG technology is designed for manufacturing size and cost scalability to moderate panel sizes (Gen 4.5 – 730 mm x 920 mm), and is targeted to fill the sub-micron design rule gap between conventional FPD backplane technologies and CMOS. Demonstrations herein are performed on SEMI-standard 150 mm substrates, but only process flows, both SiOG substrate and TFT device fabrication, are considered that are deemed scalable to FPD manufacturing.

The TFTs fabricated in this study employ active silicon layer thicknesses ranging from 220 nm to 100 nm, with an objective of achieving consistent performance at 50 nm for the purpose of enabling sub-micron devices in the future. Of critical importance are the differences in source / drain dopant implantation and activation conditions for single-crystal versus polycrystalline silicon thin films. A process is described below which addresses these differences to minimize silicon sheet resistance. SiOG wafers are processed under the same conditions in parallel with silicon-on-insulator (SOI) substrates, both wafers and device fabrication, for comparison of material performance.

Sample Preparation

SiOG Fabrication: 150 mm diameter SiOG wafers were prepared starting with (100) p-type (6-8 Ω-cm), CZ-grown silicon wafers as the donor substrates. Dry thermal oxide layers were grown with thicknesses varying from 10 nm to 100 nm, depending on the specific device configuration. Additional films may be deposited by plasma-enhanced chemical vapor deposition (PECVD), reactive magnetron sputtering (RMS), or other deposition methods. The wafers were then subjected to hydrogen ion implantation (H_2^+) at a typical energy of 70 keV and dose of 2.75x10^{16}/cm^2. Handle substrates are Corning® Lotus NXT™ wafers. Again, depending on particular device configuration, additional thin films may be deposited by the methods listed above. The wafers were prepared for bonding by brush cleaning with dilute SC1 chemistry in a spin processor to create hydrophilic surfaces. Wafer were then brought into proximity, contact is initiated, and hydrophilic bonding was achieved. Film transfer from the donor to the handle substrate was accomplished by thermally ramping in a box or tube furnace under an inert atmosphere until exfoliation of the active silicon layer occurred, typically between 450 °C and 500 °C. The transferred silicon films are thinned via reactive ion etching in fluorine-based chemistry to the target thickness, followed by a dehydrogenation cycle to fully recover the native p-type polarity and resistivity. SOI wafers with 200 nm thick buried oxide layers were fabricated alongside the SiOG wafers as control samples, particularly with identical silicon film thinning and dehydrogenation processes.

Device Fabrication: PMOS, accumulation mode, devices were fabricated utilizing a four-mask process. Silicon islands were defined through photolithography and subsequently etched via reactive ion etching (RIE). A gate insulator (GI) layer of either 50 nm or 75 nm SiO_2 was deposited using an AMAT P5000 plasma-enhanced chemical vapor deposition (PECVD) system. Subsequently, a 300 nm molybdenum layer was deposited onto the GI at 50 °C using an AMAT sputter system, followed by photolithographic patterning to form the top gate electrode. A screen oxide layer of 75 nm or 50 nm thickness was deposited on the gate prior to source/drain dopant implantation to conserve total oxide thickness. Fluorine and boron ions were implanted into the source/drain regions, with the channel area protected by the top gate; implantation energy and dose parameters were optimized based on varying silicon thicknesses (described in more detail below). Following implantation, a 200 nm SiO_2 interlayer dielectric (ILD) was deposited. Devices underwent annealing in a furnace tube at 600 °C for two hours in nitrogen to activate doping. Contact vias for the gate and source/drain regions were patterned via photolithography and etched using a 6:1 buffered oxide etch (BOE) solution. An aluminum layer of 400 nm was then deposited and patterned to serve as the contact electrodes. Finally, the devices were subjected to a post-metallization anneal at 425 °C for 30 minutes in forming gas to enhance source/drain contact quality.

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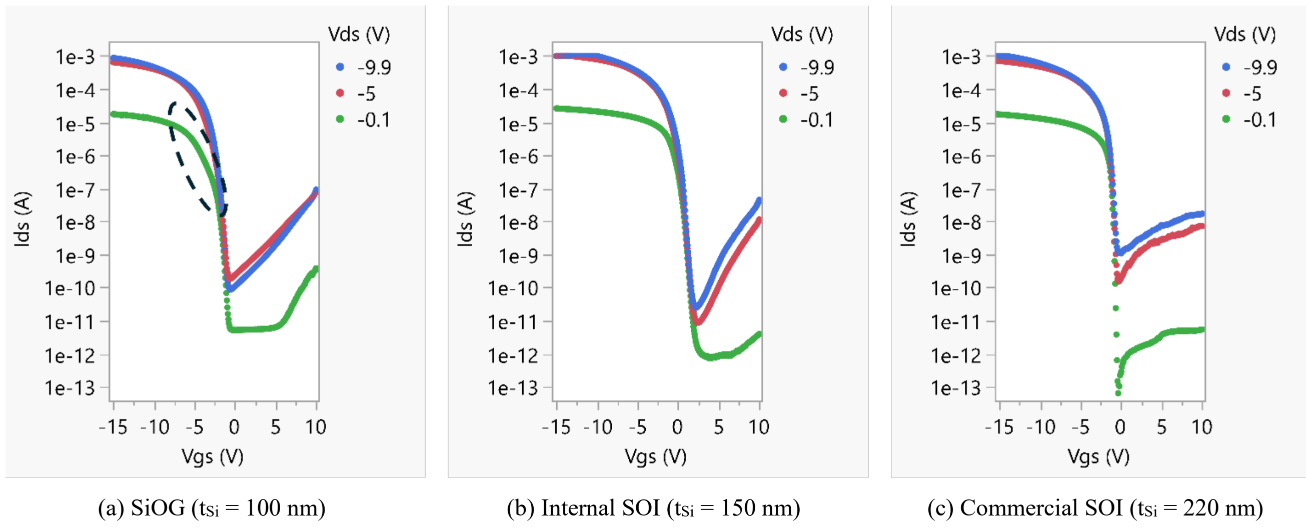

(a) SiOG (t_{Si} = 100 nm) (b) Internal SOI (t_{Si} = 150 nm) (c) Commercial SOI (t_{Si} = 220 nm)

Figure 1. TFT transfer curves for representative devices from the three sample sets. The reduced mobility of SiOG relative to SOI in this case is related to the trap state observed in the low-drain voltage SiOG transfer curve.

Following substantially the same process as the SiOG wafers, TFTs were also fabricated on the internally produced SOI wafers (150 nm silicon, 200 nm buried oxide), as well as on commercially manufactured SOI wafers with active silicon layer thickness of 220 nm and buried oxide thickness of 2 µm. One notable difference is the prime-grade surface morphology of the commercial SOI wafers as compared to the RIE-thinned, as-transferred surface morphology of the SiOG and internal SOI wafers. All SOI wafers were processed in the same manner as the SiOG wafers, most notably with the limited thermal budget to simulate FPD processing conditions.

TFT Results

Device Testing and Performance: The device dimensions ranged from L/W = 24/24 µm to 3/2 µm, and various sizes were chosen and measured for this study. The transfer curves of the TFTs, I_{ds}-V_{gs}, were obtained by sweeping the gate voltage from -20 V to 10 V, with drain biases of -0.1 V, -5 V, and -10 V applied, while grounding the source. Table 1 provides representative data, field effect mobility, sub-threshold slope, threshold voltage, and drain-induced barrier lowering (DIBL) for the three sample types, It should be noted that the simple, four-mask TFT structure used here did not employ a lightly-doped drain (LDD) structure, and thus exhibits a pronounced gate-induced drain leakage (GIDL) effect. GIDL is not a material defect; it is a transistor design-related phenomenon caused by band-to-band tunneling at the drain edge under high gate bias.

Table 1. Summary of TFT Performance

Parameter	SiOG	Internal SOI	Commercial SOI
$\mu_{h,fe}$ (cm^2/Vs)	172	263	223
SS (mV/dec)	240	312	94
V_{th} (V)	-1.77	0.78	-1.10
DIBL (V/V)	0.029	0.016	0.023

Source / Drain Doping Study

Due to differences in grain boundary presence, dopant implantation and activation are expected to vary between SiOG and LTPS. The baseline process developed for SiOG and SOI with an active silicon thickness of ≥ 150 nm uses a F_{19}^+ pre-amorphization implant ($3x10^{15}/cm^2$) at 75 keV, followed by a B_{11}^+ dopant implant ($4x10^{15}/cm^2$) at 35 keV, and thermal annealing for 2 hours at 600 °C to effectively incorporate the boron through solid phase crystallization. Using this approach, the devices shown in Figure 1 typically achieve source/drain sheet resistances of approximately 135 Ω/☐. This process was used for the internal SOI TFTs with 150 nm silicon and for the thicker 220 nm silicon in the commercial SOI wafers. To migrate to progressively thinner layers, however, requires further optimization of implant conditions. Tables 2 and 3 show the experimental matrix carried out for 100 nm and 50 nm silicon film thicknesses respectively.

Table 2. Summary of S/D Doping for 100 nm silicon film.

#	Screen Oxide Thickness (nm)	F_{19}^+ Energy (keV)	B_{11}^+ Energy (keV)	Sheet Resistance (Ω/☐)
1	100	75	35	340
2	125	75	27.5	180
3	125	50	35	380
4	125	50	27.5	1.4K

Table 3. Summary of S/D Doping for 50 nm silicon film.

#	Screen Oxide Thickness (nm)	F_{19}^+ Energy (keV)	B_{11}^+ Energy (keV)	Sheet Resistance (Ω/☐)
1	100	75	27.5	> 20K
2	100	75	20	---
3	100	50	27.5	1K
4	100	50	20	1.25K

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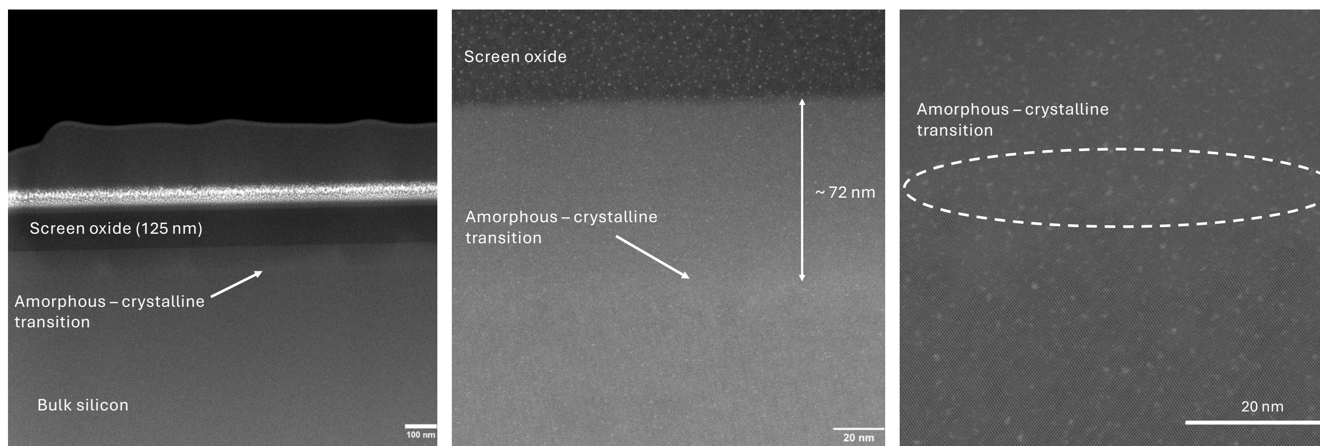

(a) 73kX magnification. (b) 580kX magnification. (c) 1650kX magnification.

Figure 2. HAADF-STEM images of bulk silicon control samples for the 75:keV F_{19}^+ / 27.5 keV B_{11}^+) implant condition, showing complete amorphization to a depth of ~ 70 nm.

Wafers for this experiment were prepared in the same manner as the TFT wafers except for further etching to obtain the thinner films. Bulk silicon wafers were also included for analysis purposes. The standard conditions used above, scaling for film thickness, should result in ~ 200 Ω/☐, but is approximately 70% greater at 340 Ω/☐. Reduction in boron implant energy results in a more favorable distribution, even improving to 180 Ω/☐, the conditions used for the SiOG TFTs in this work.

For 50 nm thick silicon films, the 100 nm optimal conditions produced extremely high resistance, and was not improved by further changes to the boron depth. Improved conditions were obtained by reducing the fluorine energy to 50 keV. Scaled sheet resistance should be in the 350 – 400 Ω/☐ range, so the best result of 1KΩ/☐ here is reasonable but not yet optimized. Examination of the series of HDAAF-STEM images in Figure 2 show that the silicon film appears completely amorphized to a depth of 70 – 75 nm, allowing the remaining 25 – 30 nm of crystalline silicon to effectively template the solid phase crystallization and boron incorporation. The same conditions for the 50 nm films would destroy the template completely. SRIM/TRIM simulations agree with this conclusion and predict a reduction is projected range for the fluorine distribution from a depth of 163 nm to 113 nm for implant energies of 75 and 50 keV, respectively. Further experimentation is required to fully optimize these conditions for 50 nm films. To further demonstrate FPD compatibility of SiOG, alternatives to the high thermal budget dopant activation above were investigated. Rapid thermal processing (RTP) demonstrated that the same sheet resistances can be achieved for 100 nm films with FPD-compatible thermal budgets:

- 8 minutes at 550 °C
- 6 minutes at 575 °C
- 2.5 minutes at 600 °C.

Impact

These results provide confidence that SiOG, as a substrate technology can deliver the inherent benefit of grain boundary elimination, enabling flat panel processing to advance well into the sub-micron regime – provided development keeps pace with panel-size photolithography [3]. CMOS backplanes for high resolution micro-displays are tied to mature technology nodes and are unlikely to see dramatic cost reductions. While AOS suffers from fundamental mobility limits, and LTPS faces worsening uniformity due to grain boundaries as pixels shrink, SiOG stands out. In the 1500 to 2500 ppi resolution range, SiOG offers a compelling combination: cost advantages from panel-level processing, and enhanced mobility and uniformity compared to incumbent backplane technologies. This positions SiOG as a strong candidate for the next generation of high-resolution displays.

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