## TFT Technology:

# Advancements and Opportunities for Improvement

For flat-panel display backplane applications, oxide TFT technology has transitioned from a disruptive challenger to a maturing competitor with respect to a-Si:H and LTPS. Here, we explore the most recent developments and the best options among the offerings.

*by* John F. Wager

**COMMERCIAL FLAT-PANEL DISPLAY BACKPLANE OPTIONS** are currently limited to three thin-film transistor (TFT) technologies: hydrogenated amorphous silicon (a-Si:H), low-temperature polysilicon (LTPS), and oxide.[1,2] As **Table 1** indicates, each technology brings a trade-off. From the perspective of this simple blue thumbs-up (good), red thumbs-down (bad), gray thumbs-sidewise (intermediate) rating system, oxide TFTs appear to come out on top. However, the true story is a bit more complicated.

Oxide is listed after a-Si:H in **Table 1**, because a-Si:H and oxide properties are more strongly correlated than those of LTPS. This a-Si:H and oxide property correlation occurs primarily because of their common amorphous microstructure, in contradistinction to the polycrystalline microstructure of LTPS. Having an amorphous microstructure leads to lower cost and the ability to scale to larger-sized glass substrates, namely Generation (Gen) 8+. Lower cost and ability to scale are the two essential advantages that make the case for choosing an a-Si:H or oxide backplane.

But why choose LTPS if it's costly and doesn't scale? On-current performance is almost always the reason. A higher on current leads to faster switching and means that a smaller TFT can be used. A smaller TFT has less parasitic capacitance, which further improves switching speed and also reduces power consumption. It also leads to a higher aperture ratio in an LCD display, thus reducing backlight power consumption. The higher on current of LTPS allows for peripheral circuit integration, thereby reducing the need to mount external silicon ICs around the display edge for row and column driver functions. These considerations mean that LTPS is an optimal backplane choice for small- and medium-sized mobile applications that require high-resolution displays.

Another distinguishing LTPS advantage is the availability of complementary metal-oxide-semiconductor (CMOS) technology that employs both n- and p-channel TFTs. To date, I would argue

*Table 1.*

Backplane technology comparison. All figures are courtesy of the author unless otherwise noted.

| PROPERTY | a-SI:H* | OXIDE | LTPS |
|---|---|---|---|
| Cost | 👍 | 👍 | 👎 |
| Scalability | 👍 | 👍 | 👎 |
| On current | 👎 | 🤜 | 👍 |
| Off current | 🤜 | 👍 | 🤜 |
| CMOS | 👎 | 👎 | 👍 |

** Here, a-Si:H = amorphous silicon; CMOS = complementary metal-oxide-semiconductor; and LTPS = low-temperature polysilicon.*

*Fig. 1.*

Still image from an animation video highlighting attributes of Corning Astra Glass, a new product developed for oxide thin-film transistor (TFT) applications.

that CMOS is not the flat-panel display backplane game-changer that it was for silicon-integrated circuit technology. Rather, the availability of CMOS means that a designer can choose to use an n-channel metal oxide semiconductor (NMOS), p-channel (PMOS), or both n-and p-channel (CMOS) TFTs. For example, PMOS appears to be preferred in LTPS OLED mobile applications, because of its top-emission architecture compatibility, better bias stress stability (compared to NMOS), and simpler process complexity (two less masks than CMOS).[3]

Careful assessment of **Table 1** reveals that oxide technology has one important distinguishing advantage compared to a-Si:H and LTPS: a low off current. Oxide TFTs employ amorphous indium gallium zinc oxide (a-IGZO) and other types of amorphous oxide semiconductors as channel layers. These oxides are unipolar, supporting electron transport, but not hole transport. In contrast, a-Si:H and LTPS are bipolar semiconductors, accommodating both electron and hole transport.

When attempting to turn a bipolar semiconductor off by applying a depleting gate bias, current first decreases with the depletion of majority carriers, but then grows as the result of an increasing density of minority carriers. This means that the off current in a TFT fabricated using a bipolar semiconductor such as a-Si:H or LTPS can never be as small as the off current obtained when a-IGZO or a similar amorphous oxide semiconductor is used. It turns out that oxide TFT off current can be orders of magnitude smaller than that of an a-Si:H or LTPS TFT. This translates into reduced power dissipation for oxide TFT technology.

*Fig. 2.*

Generation (Gen) 4.5 semi-dynamic physical vapor deposition (PVD) cluster tool for oxide TFT manufacturing. This system features a rotary array deposition source and horizontal substrate movement for improved uniformity.

Figure 1: Courtesy of Corning, Inc.

## SIZE MATTERS

How does one decide between the three flat-panel display backplane options? The a-Si:H technology is mature, predictable, and available. If your application is not too demanding and cost is a critical consideration, choose a-Si:H. Thus, selecting oxide or LTPS usually means that a-Si:H is inadequate in terms of performance for your application.

Selecting between oxide and LTPS boils down to a glass size consideration. As noted in **Table 1**, oxide technology readily scales to large glass substrate sizes, Gen 8+. Thus, oxide TFTs dominate large-area applications such as OLED TVs in which a-Si:H can't deliver the required performance. Large-area scaling is a tremendous advantage of oxide TFT technology, because moving to a larger glass substrate size is the most straightforward approach for reducing cost.

Corning's announcement of Corning Astra Glass **(Fig. 1)** is an exciting recent development for oxide TFT technology, because it's targeted specifically at the oxide TFT market. The 725 °C strain point of Corning Astra Glass is intermediate to that of Corning EAGLE XG Glass (669 °C) and Corning Lotus NXT Glass (752 °C), primarily servicing a-Si:H and LTPS technologies, respectively. Glass substrate availability is a key consideration when scaling beyond Gen 10 dimensions, given the trend toward colocation of glass substrate and flat-panel display manufacturing facilities.[4] In a Gen 10+ fabrication plant (fab), the glass size is so large that shipping glass substrates from a remote glass manufacturing plant is no longer practical.

Because excimer laser annealing and ion implantation are required for LTPS manufacturing, scaling LTPS beyond Gen 6 tends to be challenging and expensive. Thus, the sweet spot for LTPS applications is small- or medium-area high-performance applications such as cellphones. However, the inability to readily scale to a large glass substrate size is a serious liability, because it takes away the most direct path toward future cost reduction. Furthermore, the need for nonmainstream and hard-to-scale

processes such as excimer laser annealing and ion implantation in LTPS fabrication means that the LTPS process flow distinctly differs from that of a-Si:H. In contrast, oxide and a-Si:H manufacturing processes are quite similar, so that upgrading an existing fab from a-Si:H to oxide is likely to be a straightforward and sometimes attractive option.

## UNDERSTANDING OXIDE TFT TRENDS

**Table 2** lists manufacturing facilities and institutions that offer foundry and/or developmental services for oxide TFTs. It is evident that oxide TFT manufacturing capability continues its rapid ramp up. Almost all of the activity under construction or ramping up (green) and planned (red) is directed toward large Gen 8+ fabs. Most reports are vague regarding how much of a facility's capability is to be devoted to oxides, which makes it difficult to specify total oxide TFT manufacturing capability. It is encouraging to see foundry and developmental service availability; this indicates that oxide TFT technology is beginning to mature.

**Fig. 2** illustrates an example of the new manufacturing tools being developed to support oxide TFT technology. This semi-dynamic physical vapor deposition (PVD) cluster tool is targeted for Gen 4.5 applications. It's suitable for R&D activities constrained to a small footprint, and yet it's scalable to Gen 6 glass substrate sizes, as required for the support of mobile applications. Its semi-dynamic platform provides mura-free oxide films, based on a proven rotary PVD architecture. Additionally, the PVD tool design strategy employed makes it easy to control plasma ignition and the nature of ion bombardment for the realization of low-defect, high-quality thin films.

Post-deposition annealing of the sputtered amorphous oxide semiconductor channel layer in oxygen or in an oxidizing ambient is a critical step in oxide TFT manufacturing, typically defining the maximum process temperature. Recall that the strain point of Corning EAGLE XG Glass (a-Si:H), Corning Astra Glass (oxide), and Corning Lotus NXT Glass (LTPS) are 669, 725, and 752 °C, respectively, while the a-Si:H TFT maximum process temperature is ~350 °C. Thus, simple scaling with respect to strain point suggests that the maximum process temperature for oxide and LTPS TFT fabrication are ~400 and ~430 °C, respectively. This observation is interesting for two reasons. First, because the glass price usually increases with the increasing strain point, it's likely that oxide glass substrates are more expensive than those of a-Si:H, but less expensive than those of LTPS. Second, although in the early days of oxide TFT development there was a tremendous push to keep the annealing temperature below 350 °C (and thus interchangeable with a commercial a-Si:H process) and there are many reports in the literature of successful oxide TFT processing at much lower temperatures (even room temperature), it appears that optimal oxide TFT processing requires an annealing temperature in excess of 350 °C.

Why is post-deposition annealing of the oxide TFT channel layer required? The easy answer is that TFT performance demands it in terms of obtaining optimal electron mobility, subthreshold slope, turn-on voltage, and device stability. The scientific answer to this question is more difficult to ascertain and is open to debate. I suspect that annealing helps to heal sputter-induced damage of the as-deposited film, and that the oxidizing ambient minimizes the oxygen vacancy concentration.

**QUICK TAKE**

Oxide TFTs dominate large-area applications such as OLED TVs in which a-Si:H can't deliver the required performance. Large-area scaling is a tremendous advantage of oxide TFT technology because moving to a larger glass substrate size is the most straightforward approach for reducing cost.

Additionally, post-deposition annealing usually increases the oxide thin film's density (from perhaps 93 to 96 percent). Obtaining a fully-dense channel layer is a key aspect of optimizing oxide TFT performance and stability. As an aside, the density of a solution-processed thin film is typically less than 90 percent (and often less than 80 percent), presenting a serious challenge that's likely to preclude commercialization of such films for many electronic applications.

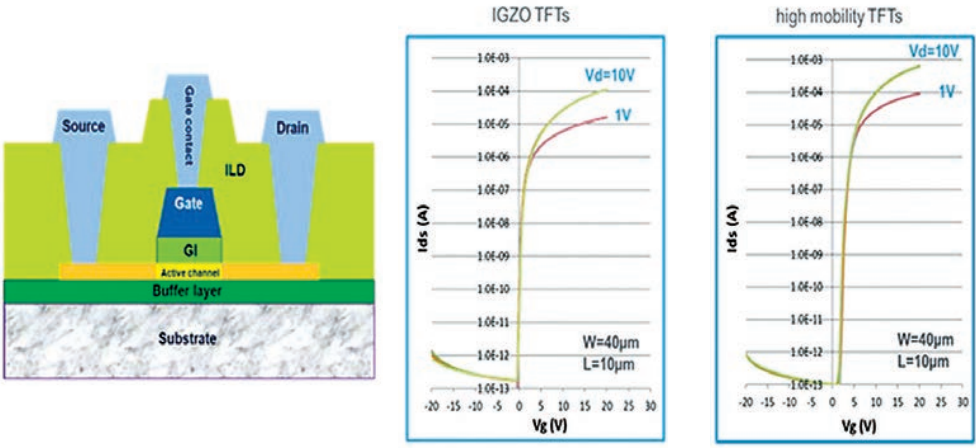
**Fig. 3** pertains to recent state-of-the-art oxide TFT device

***Table 2.***

Oxide TFT manufacturing and foundry or development facilities (blue = in operation, green = under construction ramping up, and red = planned).[4–14]

| MANUFACTURING FACILITY | FAB SIZE |
|---|---|
| BOE (B17)—Wuhan, China (a-Si:H TFT/oxide + WOLED*) | Gen 10.5 |
| China Star (T7)—Shenzhen, China (a-Si:H TFT/oxide + WOLED) | Gen 10.5 |
| Mantix Display Technology—Putian, China (a-Si:H/oxide TFT) | Gen 6 |
| Foxconn/SDP—Kameyama, Japan (oxide TFT) | Gen 6 |
| Foxconn/SDP—Kameyama, Japan (oxide TFT) | Gen 8 |
| LG Display (E2)—Paju, South Korea (LTPO) | Gen 4.5 |
| LG Display (P8)—Paju, South Korea (oxide TFT) | Gen 8.5 |
| LG Display (P9)—Paju, South Korea (oxide TFT) | Gen 8.5 |
| LG Display—Guangzhou, China (oxide TFT) | Gen 8.5 |
| LG Display (P10)—Paju, South Korea (oxide TFT) | Gen 10.5 |
| Panda—Nanjing, China (oxide TFT) | Gen 8.5 |
| Panda—Chengdu, China (oxide TFT) | Gen 8.6+ |
| Royole—Shenzhen, China (oxide + OLED) | Gen 5.5 |
| Samsung (A2)—Asan, South Korea (LTPO) | Gen 5.5 |
| **Foundry or development facility** | |
| dpiX—Colorado Springs, Colorado | |
| Flexible Electronics & Display Center—Tempe, Arizona | |
| Holst Centre—Eindhoven, Netherlands | |
| Semiconductor Energy Laboratory—Kanagawa, Japan | |

** LTPO = low-temperature polycrystalline silicon and oxide; WOLED = white OLED; SDP = Sharp Display Products Corporation*




| Electrical Parameters | IGZO channel | high mobility channel |
|---|---|---|
| Vth (V) @Id = (W/L) x1E-9 (A) | 0.5 | 2.5 |
| SS (V/decade) | 0.17 | 0.18 |
| $\mu_{FE}$ ($cm^2$/Vs) @Vg=Vth + 10V, Vd=1V | 12.3 | 64.3 |
| $I_{OFF}$ (A) @Vg=-7V, Vd=10V | < 1E-12 | < 1E-12 |
| PBTS (V) @Vg=+30V, 60C, 1hr | < 0.5 | 2 ~ 3 |
| NBTS (V) @Vg=-30V, 60C, 1hr | < 0.1 | < 0.1 |

***Fig. 3.***

Performance summary for self-aligned top-gate oxide TFTs. IGZO = indium gallium zinc oxide; NBTS = Negative Bias Temperature Stress; and PBTS = Positive Bias Temperature Stress.

performance. Two types of self-aligned top-gate oxide TFTs are compared. This (in and of itself) is a notable advance, for three reasons. First, oxide TFTs were initially fabricated using a bottom-gate architecture. In many respects, a top-gate oxide TFT is a more challenging device to build. Thus, top-gate TFT realization—using a commercial tool—is strong evidence that oxide TFT technology indeed is maturing. Second, obtaining an oxide TFT that's both top-gate and self-aligned means that its parasitic capacitance is reduced, which improves switching speed and reduces power consumption. Third, because the amorphous oxide semiconductor surface inherently is protected in a top-gate TFT structure, its device stability likely is enhanced.

Assessment of **Fig. 3** reveals several other interesting oxide TFT trends. The two TFTs compared in **Fig. 3** differ in the nature of their channel layer (for example, the IGZO and high mobility channel layers). Previously, IGZO and oxide TFT were considered to be terms that could be used interchangeably. It's clear from **Fig. 3** that this is no longer true; amorphous oxide semiconductors other than IGZO will likely be employed soon in products. Electron mobility is, to a large extent, the driving force promoting the use of alternative amorphous oxide semiconductors, as revealed by the factor of 5x improvement in the field-effect mobility (see **Fig. 3**). The red color coding in **Fig. 3** warns that more work is required with respect to improving the positive bias temperature stress (PBTS), however, before these high-mobility TFTs are ready for commercial implementation.

**Fig. 4** provides channel length scaling data for a high-mobility oxide TFT.[15] Drain current versus gate voltage transfer curves are well-behaved, showing virtually no shift in either turn on or threshold voltage for gate lengths between 3 to 10 μm. Thus, there is no evidence of short-channel behavior for a gate length as small as 3 μm. Furthermore, the measured resistance versus channel length trend displays a common intersection point at 0.77 μm, the channel length correction, allowing assessment of the effective channel length. Collectively, the two plots included in **Fig. 4** provide more ammunition for the assertion that the high-mobility oxide TFT is of high quality.

## THE DREAM IS OVER

Many years ago—before oxide TFT technology was a commercial reality—I and many others began to dream of an oxide TFT CMOS-like technology.[16] Why CMOS? The CMOS circuit design strategy was revolutionary in the evolution of silicon-integrated circuits. CMOS technology offers low-power consumption, low heat dissipation, high packing density, simple circuit architecture, large noise margin, and straightforward paths toward the design of analog and digital circuits, even on the same chip. As mentioned previously, CMOS is an essential advantage for LTPS, at least in applications that require CMOS. These silicon technology CMOS historical considerations prompted many researchers to recognize the potential worth of an oxide TFT CMOS-like technology.

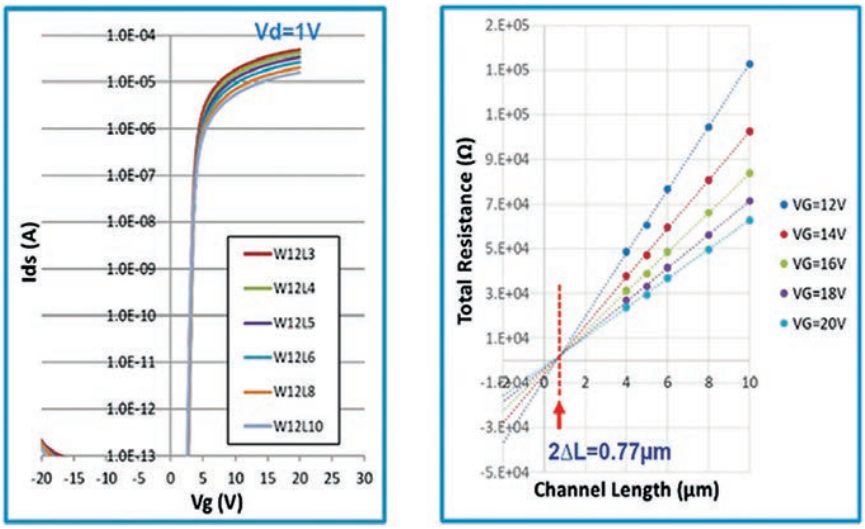
So, what's the problem with oxide TFT CMOS? It turns out that developing a p-type oxide with a performance similar to that of a-IGZO or other n-type amorphous oxide semiconductors is an extraordinary challenge, and (I think) probably impossible. The best p-type oxide candidates to date are (arguably) copper oxide (Cu2O) and tin monoxide (SnO).[17] These oxides are polycrystalline, not amorphous, which doesn't bode well for future scaling to large glass substrate sizes. Their electrical performance and TFT stability are poor. Combining either of these p-type oxides with a-IGZO to realize oxide TFT CMOS would be a process integration nightmare. Oxide TFT CMOS off-current performance would be abysmal, because of the invariably large leakage current of the p-type oxide TFT, thereby negating a key advantage of n-type oxide TFT technology. Thus, I am (regrettably) no longer a believer in the possibility of achieving a viable oxide TFT CMOS technology.

Figures 2, 3, 4: Courtesy of Jung Bae Kim of Applied Materials, Inc.

## IS LTPO A NEW DREAM?

Technological advance is a funny thing. Just when you give up on a dream, something vaguely similar shows up. That's how I view low-temperature polycrystalline silicon and oxide (LTPO).[18] Here's the basic idea: Oxide TFT technology gives you a great switch with excellent off-current performance, while LTPS offers optimal on-current performance, and CMOS to boot. If these two technologies are combined, we obtain the best of both worlds (this would lead to three blue thumbs-up at the bottom of **Table 1**) in terms of pixel switching and peripheral circuit integration. Of course, this merger of oxide and LTPS technologies is an exceedingly complicated manufacturing challenge and comes at a great cost (literally) and lack of scalability to large glass substrate sizes.

A technology such as LTPO only makes sense if an appropriate "killer app" can be identified. To date, Apple (the inventor of LTPO) has employed it in the Apple Watch Series 4. From my perspective, this certainly qualifies as an "app," but I'm not sure about the "killer" part. Things may change, however, as the internet is abuzz with rumors that Apple may soon offer an LTPO iPhone. It will be interesting to see if this LTPO iPhone development actually occurs; and if so, whether its emergence indeed puts the "killer" in "app."




*Effective Channel Length = Mask Channel Length - Channel Length Reduction (2ΔL)*

***Fig. 4.***

Channel length scaling and effective channel length calculation using the transmission-line method from self-aligned top-gate oxide TFTs with high-mobility channels.

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