

# PROGRESS AND APPLICATION OF THROUGH GLASS VIA (TGV) TECHNOLOGY

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## ABSTRACT

Glass provides many opportunities for advanced packaging. The most obvious advantage is given by the material properties. As an insulator, glass has low electrical loss, particularly at high frequencies. The relatively high stiffness and ability to adjust the coefficient of thermal expansion gives advantages to manage warp in glass core substrates and bonded stacks for both through glass vias (TGV) and carrier applications. Glass also gives advantages for developing cost effective solutions. Glass forming processes allow the potential to form both in panel format as well as at thicknesses as low as 100  $\mu\text{m}$ , giving opportunities to optimize or eliminate current manufacturing methods.

As the industry adopts glass solutions, significant advancements have been made in downstream processes such as glass handling and via/surface metallization. Of particular interest is the ability to leverage tool sets and processes for panel fabrication to enable cost structures desired by the industry. Here, we provide an update on advancements in these areas as well as handling techniques to achieve desired process flows. We also provide the latest demonstrations of electrical, thermal and mechanical reliability.

Key words: Through glass via (TGV); glass; panel

## INTRODUCTION

New initiatives in semiconductor packaging have created needs for new materials solutions. There has been substantial effort to extend interposer technology for 3D-IC stacking. Multiple solutions are being developed to address some of these needs including traditional interposers utilizing various commonly used materials as well as Fan-Out Wafer Level Packaging (FOWLP), which has become a popular consideration in attempt to achieve lower cost. [1] Furthermore, the proliferation of mobile devices and the Internet of Things (IoT), leads to increasingly difficult requirements in RF communications. These include such requirements as the introduction of more frequency bands, smaller/thinner package size and need to conserve power to increase battery life as new functionality is introduced. Glass has proven to be an excellent solution to these challenges. [2]

Glass has many properties that support the initiatives described above. These include high resistivity and low

electrical loss, low or adjustable dielectric constant, and adjustable coefficient of thermal expansion (CTE). There has been much work in recent years as researchers demonstrate leveraging glass properties to achieve these objectives [3]-[6].

In order to leverage glass for many RF and interposer applications, it is often necessary to have precision vias for electrical interconnect and other functional purpose. The ability to put precision holes in glass and downstream metallization to create these vias continues to mature towards volume manufacture. Work in recent years has also demonstrated the reliability of these structures in glass [7]-[9].

Over the past several years at Corning Incorporated, there have been significant advances in the ability to provide high-quality vias in glass substrates of various formats. Examples are shown in Fig.1. The process employed provides the opportunity to leverage both through and blind vias in both wafer and panel format. The glass substrates with holes have been shown to give strength on par with bare glass, and filled vias have been shown to have excellent mechanical and electrical reliability after thermal cycle tests [9]-[11]. The approximate current best practice capabilities are summarized in Table 1 below. These represent guidance for the current TGV process, but in many cases the capabilities can be extended.



1a: Through Glass Vias

1b: Blind Glass Vias

**Fig. 1:** Examples of both through glass vias (TGV) and blind glass via (BGV).

In addition to enhanced technical performance, packaging solutions must also be cost effective. Glass forming processes such as Corning's fusion forming process, gives the ability to form high quality substrates in large formats ( $>> 1 \text{ m}$  in size). The process can be scaled to deliver ultra-slim flexible glass to thicknesses down to  $\sim 100 \mu\text{m}$ . Providing large substrates in wafer or panel format at 100  $\mu\text{m}$  thickness gives significant opportunities to reduce manufacturing costs. The advantages given by Corning's fusion forming process for supplying substrates for

electronics applications, has been previously reported [7], [8].

**Table 1.** TGV specification

Attribute	Current Capability*
Outer Diameter (OD)	25 – 100 $\mu\text{m}$
Minimum Pitch	$\sim 2\times$ OD
Type	Through and Blind
Wafer Size	Up to 300 mm
Panel Size	Up to 515 x 515 mm
Thickness (mm)	0.1 – 0.7

\*Approximate.

## II. Glass Material Properties

### A. Adjusting the CTE for Carrier and Interposer Applications

Glass material properties are determined by the specific chemical make-up of the glass, making it possible to tailor glass composition to achieve a targeted CTE; thus enabling management of stack warp. Previously, we have shown examples of the material properties of two fusion formed glass types, in which it is possible to achieve very different CTE values while maintaining similar mechanical properties [7].

One of the important challenges in 3DIC stacking is reliability due to CTE mis-match and glass provides an excellent opportunity to manage warp of 3D-IC stacks but optimizing CTE. [6] Figure 2 gives an illustration of the challenge of stacking substrates with multiple CTE in an interposer application. Figure 2a schematically shows Si chips mounted on a Si interposer, which is then mounted on an organic substrate. The CTE mismatch causes failures when the substrates go through temperature cycles. However, if instead of a Si interposer, a glass interposer with CTE in between glass and organic is used, this warp can be better managed and increased reliability realized as demonstrated in work at Georgia Tech’s Packaging Research Center (PRC) and illustrated Fig. 2b. [6]



**2a:** CTE mis-match creates reliability challenges.

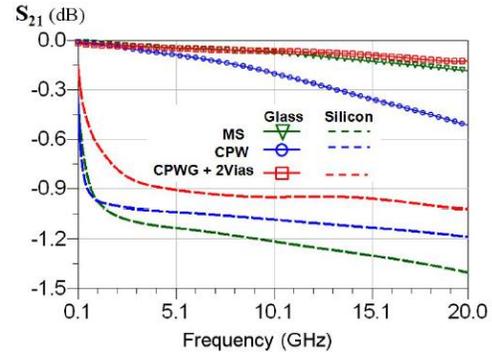
**2b:** Utilizing the ability to adjust the CTE of glass helps to manage warp and improve reliability.

**Fig. 2:** Illustration of CTE mismatch in 3DIC stacking.

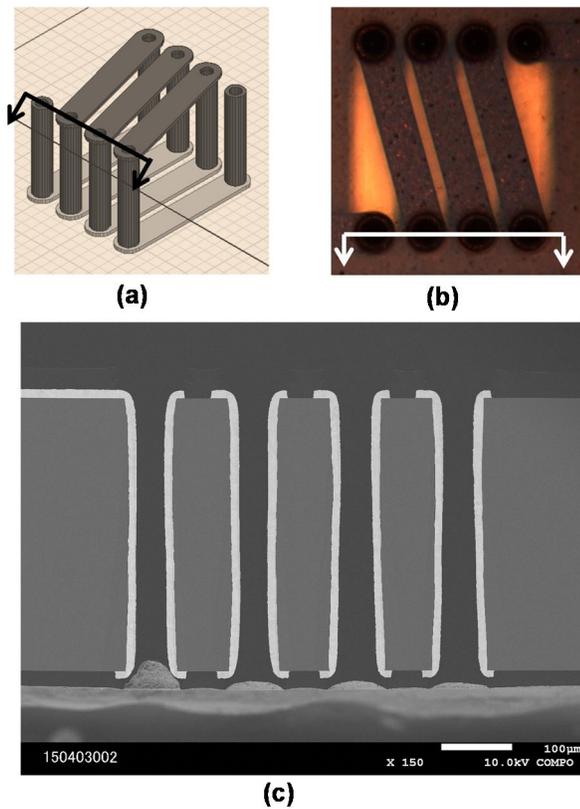
### B. Electrical Performance

As new, higher frequencies used in RF applications are released, the electrical properties of the substrates become increasingly important. As a semiconducting material, standard silicon tends to have increased loss at higher

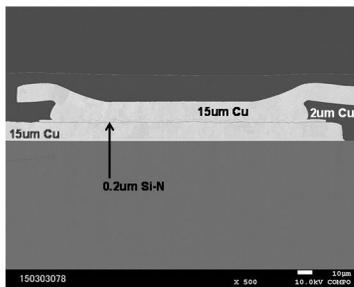
frequencies. Work done in collaboration with the Industrial Technology Research Institute (ITRI) in Taiwan illustrates this well. [16] In this work co-planar waveguides (CPW), micro-strip lines (MS) and co-planar waveguides with 2 vias were constructed on glass and silicon substrates, and impedance matched to  $\sim 50$  ohm. The structures were then tested up to 20 GHz and insertion loss was characterized. The results are shown in Fig. 3. Since glass is an insulator, there is much less loss as frequency is increased beyond a few 100’s of MHz. Given the importance of minimizing power loss at these higher frequencies coupled with the need to continue to reduce package size, glass provides valuable material for all applications working in the GHz range.



**Fig. 3** – The insertion loss ( $S_{21}$ ) from transmission lines on glass and standard silicon substrates showing much less loss in glass at higher frequencies. A good example of leveraging the insulating properties of glass is to provide high-Q inductors and capacitors in a glass-based LC network as recently described [2]. In this work, the high-Q inductors were created by utilizing solenoid inductors shown schematically in Fig. 4a. The top and cross sectional view of the fabricated inductors is shown in Figs. 4b and 4c respectively. High-Q capacitance was achieved by utilizing a metal-insulator-metal construction. Fig. 5 shows the MIM capacitor formed on the same TGV glass substrate.

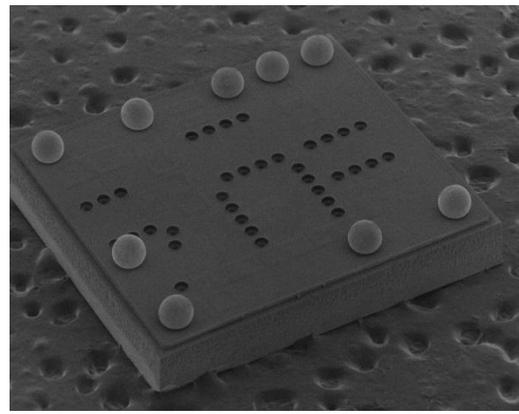


**Fig. 4.** 3D TGV inductor formation. (a) 3D rendering, (b) top-down photograph, (c) cross-sectional SEM of TGV with conformal Cu plating on the TGV sidewalls and the top & bottom sides of the glass to form a 3D TGV inductor



**Fig. 5** Cross-sectional SEM of TGV with conformal Cu plating on the TGV sidewalls and the top & bottom sides of the glass to form a 3D TGV inductor

The TGV IPD parts were mounted on evaluation boards and further tested for both electrical functionality and thermal and mechanical reliability, showing no performance degradation or any board-level reliability issues. The insulating properties of glass provide very high-Q performance.



**Fig. 6** SEM bird's eye view of completed LC networks device.

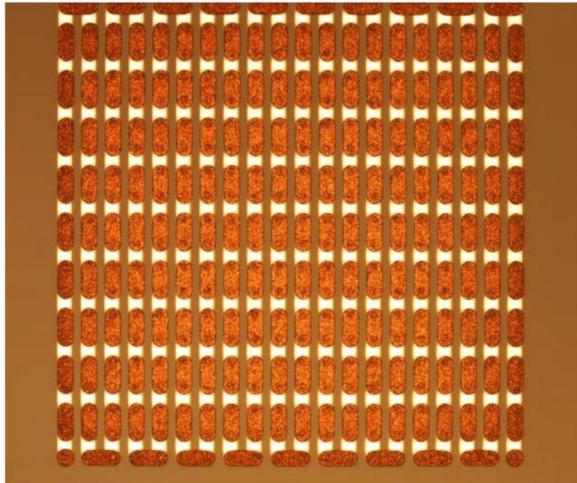
### Thermal Cycle Testing

The fabrication of thin glass interposers with Cu filled through glass vias (TGV) was done using standard back end of line (BEOL) fabrication tools with no significant modification of any of the equipment wafer handling to accommodate glass wafers. In order to test the effect of the glass CTE on the long term reliability of the glass interposers, 150 mm glass wafers formulated with two different CTEs, 3 ppm/°C and 8 ppm/°C, were used in the fabrication process.

Full thickness 150 mm glass wafers with 35 μm x 125 μm blind TGVs were sputtered with a thin adhesion layer of Ti and Cu. No barrier or additional dielectric layer were deposited in the TGVs before the metallization. Highly conformal copper seed layers were deposited using metal-organic chemical vapor deposition (MOCVD), in preparation for TGV plating. The seed layers were nominally 0.75 μm in thickness, which was uniform throughout the TGVs. Electroplating of Cu was used to fully fill the TGVs and the overburden was removed using chemical mechanical polishing (CMP). High resolution x-ray imaging was used to verify the void-free nature of the Cu fill in the TGVs. To form the TGV test structures, plated Cu routing layers were patterned on both sides of the thin wafers. These routing layers were electroplated on a sputtered Ti/Cu seed layer with no barrier covering the glass substrate. Thin wafer handling was done using 3M's Wafer Support System (WSS). More details on the fabrication of these glass interposer test vehicle wafers can be found in previously published work [9].

After fabrication was completed, wafers from each glass type were electrically tested for continuity of the daisy chain test structures. Electrical continuity testing was done on eight test arrays, randomly chosen across the diameter of four wafers. Each test array consisted of 20 x 20 TGVs on 100 μm pitch, with each of the TGVs connected in series. The TGV test chain array, an example of which is shown in Figure 7, has testing points at the front and back of every TGV, so that any electrical discontinuity can be tracked down to the single metal link or TGV. The results of the

initial round of electrical continuity testing are shown in Table 2. The combined yield of the TGVs and routing metal links was over 99.85% for both types of glass.



**Figure 7.** Optical microscope image of a TGV daisy chain test feature consisting of a 20 x 20 array of TGVs on 100 μm pitch. The topside metal links appear as copper colored and the links on the backside appear white.

**Table 2.** The results of 2-wire electrical continuity tests on 20 x 20 arrays of TGVs on 100 μm pitch

Wafer	CTE (ppm/°C)	No. of 20x20 arrays tested	Yield of TGVs & routing metal (%)
SGW3 - Wafer 1	3.2	8	99.97
SGW3 - Wafer 2	3.2	8	99.97
SGW8 - Wafer 1	8.1	8	99.72
SGW8 - Wafer 2	8.1	8	100.00

After this initial test, eight additional test arrays were selected from each type of glass with starting TGV array yields of 100%. These arrays were then subjected to thermal cycle testing, which consisted of 1000 cycles from -40°C to 125 °C with 1 hour cycle time and 15 min soak time at each temperature extreme (JEDEC JESD22-A104 condition G). An intermediate test point of 500 cycles was also done. The results of electrical testing at 0, 500 cycles, and 1000 cycles are shown in Table 3. Figure 8 shows the TGV profile after 1000 thermal cycles. Note that there is no cracking or delamination seen.

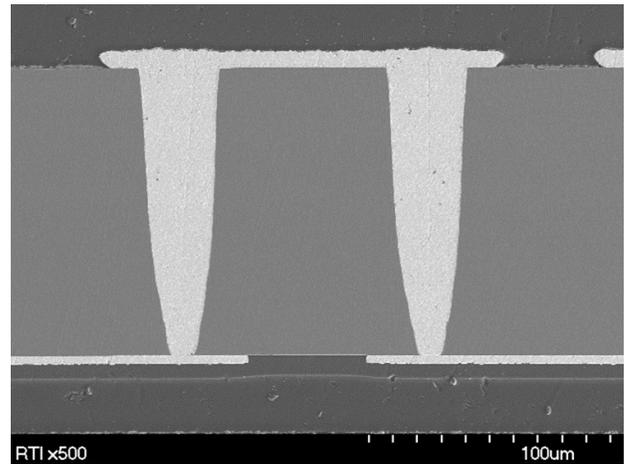
**Table 3.** The results of 2-wire electrical continuity tests on eight known-good 20 x 20 arrays of TGVs on 100 μm pitch before and after thermal cycle testing

No. of thermal cycles	Wafer	CTE (ppm/°C)	Yield of TGVs & routing metal (%)	Median chain resistance (Ω)
0 cycles	SWG3-Wafer 1	3.2	100.00	10.4

	SWG8-Wafer 2	8.1	100.00	6.7
500 cycles	SWG3-Wafer 1	3.2	100.00	15.4
	SGW8-Wafer 2	8.1	100.00	13.5
1000 cycles	SGW3-Wafer 1	3.2	100.00	16.6
	SGW8-Wafer 2	8.1	100.00	15.9

### III. Form Factor

Another valuable aspect of leveraging glass as a semiconductor packaging substrate is that the forming processes lend themselves to providing large form factors.[7], [8] This is important as the IoT will require

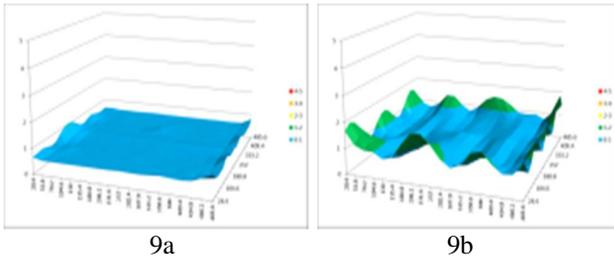


**Figure 8.** Cross section SEM image from an interposer test vehicle in SGW3 glass after 1000 thermal cycles. These were measured to be from 17 μm to 19 μm in diameter at the wafer backside and 35 μm diameter at the front side.

billions and even trillions of devices and sensors. Being able to utilize economies of scale given by panel processing is very important.

Recent work has shown significant progress in the ability to process glass panels > 500 mm in size [17]. An important outcome of this work demonstrated one advantage of using glass in this application. Specifically, that the increased stiffness and thermal stability of glass relative to current solutions results in improved flatness (See Fig. 9).

In Fig. 9a, the profile of a 508 mm × 508 mm panel size glass substrate with two layers build-up after pre-cure processes is shown. Figure 9b shows the profile of organic substrate after same processes. There is ~3 x better warpage performance for the glass based substrate. This has important implications in that the improved flatness of the glass based substrate enables finer lines and spacing for redistribution layers relative to organic substrates. This allows high performance devices to be fabricated in a panel format, which provides substantial opportunity for both cost effective and high quality solutions.



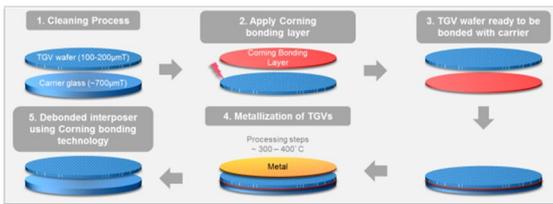
**Fig. 9:** (a) War page measurement result of glass substrate after two layers build-up (b) War page measurement result of organic substrate after build-up

In addition to scaling glass substrate size, it is possible to scale the process to deliver ultra-slim flexible glass to thicknesses down to ~100  $\mu\text{m}$  (see Fig. 10). Providing large substrates in wafer or panel format at 100  $\mu\text{m}$  thickness gives significant opportunities to reduce manufacturing costs because there is likely to be no need for grinding and polishing operations.



**Fig.10.** Manufacture of high quality ultra-slim flexible Corning® Willow® Glass provides substantial opportunities to deliver substrates for TGV that do not require post processing.

Handling of ultra-thin glass in standard wafer or panel processing operations can be a challenge. However, solutions are being developed. Corning’s Advanced Lift-off Technology (ALoT) is a carrier based solution that is designed to be compatible with high temperatures (> 450 C) without outgas, as well as maintaining compatibility with important process chemistries such as cleaning (SC1, SC2, etc.) and metallization. The process is shown schematically in Fig. 11.

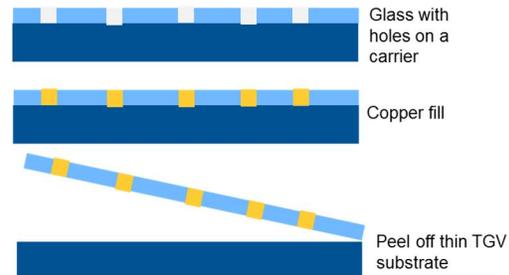


**Fig. 11.** Schematic showing an approach for handling thin glass through metallization.

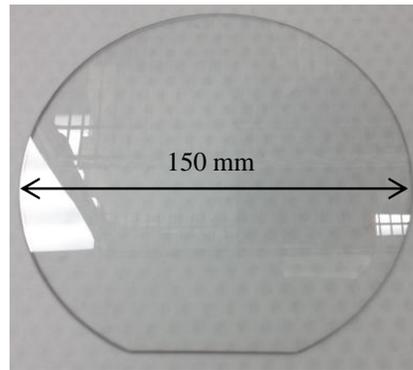
The approach is to apply a surface treatment on a glass carrier wafer to prevent permanent bond at high temperatures, while maintaining enough adhesion strength to enable via and surface metallization. The thin metallized glass TGV wafer will then be mechanically de-bonded and

processed further. This approach is relevant for wafers and panels.

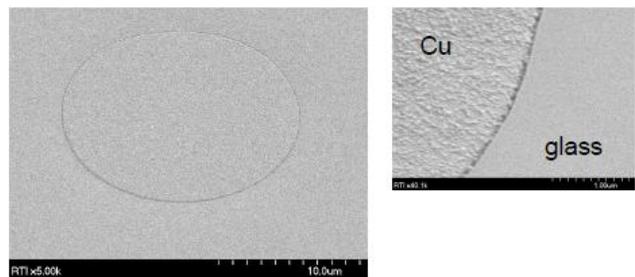
Work recently at RTI International in Research Triangle, NC has been done to demonstrate feasibility of utilizing the ALoT structure to perform metallization of the vias. Glass with 100  $\mu\text{m}$  thickness and ~30 $\mu\text{m}$  diameter through vias was provided on a carrier. RTI then applied the seed layer and via fill using a process consistent with the method used to fill blind vias.[9] However, instead of back grinding to expose the bottom of the vias, with ALoT the thin glass is peeled off mechanically as shown schematically in Fig. 12. Figure 13 shows the 150 mm bonded wafers.



**Fig. 12:** Cartoon of leveraging ALoT technology to metallize through vias in 100  $\mu\text{m}$  thick glass.

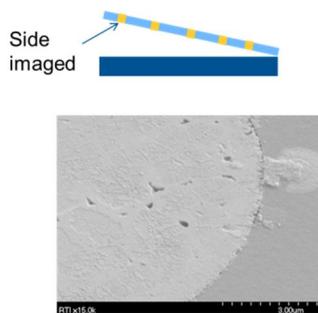


**Fig. 13:** Image 100  $\mu\text{m}$  thick glass with 30  $\mu\text{m}$  diameter vias temporarily bonded onto a glass carrier using ALoT technology.



**Fig. 14:** Cartoon of leveraging ALoT technology to metallize through vias in 100  $\mu\text{m}$  thick glass.

Figure 14 shows the result after via metallization and overburden removal from the top surface. The thin glass completed processes for via metallization, overburden removal and Chemo-Mechanical Planarization (CMP) and very good planarity of the Cu and glass surface was achieved. After completion of top surface CMP, the wafers were mechanically de-bonded and an SEM image of the TGV on the back surface was collected to evaluate the ability to achieve good planarity without any post-processing (e.g. there was no planarization of the back surface). Figure 15 shows an SEM image of the back surface TGV after de-bond. There is work to be done to achieve perfect bond and planarity, but the result shows the feasibility of using this approach to effectively fill TGV in thin glass. Optimization of this method provides exciting opportunities to dramatically enhance cost effectiveness of providing thin glass solutions by eliminating back grinding operations and enabling further downstream process optimization. Furthermore, while this demonstration was completed in 150 mm wafer format, it is scalable to 300 mm wafer and even panel formats.



**Fig. 15:** SEM image of bottom of metallized via after de-bond (no polishing).

## V. Conclusion

Glass has a number of properties that make it an exciting material for various packaging applications. The electrical performance of glass gives reduced electrical loss relative to silicon. This becomes even more important at high frequencies, which will be used for next generation mobile networks. The important implication would be the ability to increase smart phone functionality while maintaining or extending battery life.

Adjusting material properties like CTE generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications in multiple forms. Furthermore, the ability to form high-quality glass in thin, large sheets enables a number of opportunities to reduce cost. Handling technologies that provide means to effectively process ultra-thin glass are being demonstrated.

Well-formed through and blind vias have been demonstrated and existing metallization technology can be

leveraged to generate very good Cu filling performance in glass in both wafer and panel formats. Reliable performance of Cu-filled vias in glass has been demonstrated. These developments make glass an exciting material for next generation packaging applications.

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