

Glass Wafer Mechanical Properties: A Comparison To Silicon

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Introduction

The billion dollar silicon industry is built on the extreme uniformity, chemical, and mechanical strength of perfect crystals of silicon configured in the shape of a wafer for standard integrated circuit processing. Silicon is an ideal substrate for creating transistors. Thinning the silicon integrated circuit (IC) substrate has now become a common process approach to maintain the trend established by Moore's law and to meet the packaging form factor required by consumer applications. The thinned silicon wafer can be used in a stand alone thin form factor package, or combined with other thinned silicon device wafers to create a three dimensional stack IC structure (3D-IC). A thinned silicon IC wafer is very difficult to handle. Therefore it generally requires the use of a carrier substrate attached with a temporary bonding method as an aid to handling.

While it is convenient to use a known silicon wafer as a mechanical carrier wafer during process development activities for wafer thinning, it is illustrative to consider other alternatives, such as glass wafers. Glass wafers have attributes such as optical transparency that enable visible inspection and other light-based processing techniques, and innovative forming processes that minimize or eliminate fabrication steps, for example. To be considered as a drop in alternative carrier, a glass wafer needs to have similar mechanical properties as a silicon wafer. This includes form and fit to travel in and out of standard fabrication tools plus the basic materials properties required to act as a carrier.

Background

Figure 1 shows a simplified process for creating a thin silicon device wafer. Depending on the application, the final device wafer thickness may be anywhere from about 10 μm to 150 μm . If the device wafer is thinner than 150 μm it is possible to process the thin wafer through various backside process steps if the thinned wafer is on a carrier wafer.

There are several methods for accomplishing the temporary bonding process. Regardless of the temporary bonding method used, to achieve a thinned device wafer with good process control means the planarity and warp of the complete stack consisting of carrier wafer, plus temporary bonding adhesive, plus the silicon device wafer must be carefully controlled.

Thus the choice of each of the elements in the composite bonded stack is very important. Inside the processing tools there may be vacuum or electrostatic chucks to hold the combined stack flat, however in the transfer cassettes or storage boxes the wafer stack will be in a relaxed or free state resulting in warp.

Typical process temperatures depend on the specific application but may range from room temperature to 300°C. In order to control the warp of the combined stack throughout the fabrication process, the coefficient of thermal expansion (CTE) must be carefully chosen. If there is too much warp a 300 mm diameter wafer stack may not slide in and out of the cassettes or can not be clamped securely to vacuum chucks.

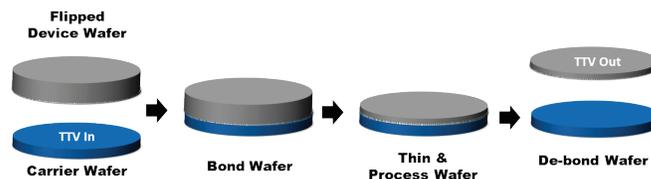


Figure 1. Use of a temporary bonded carrier for silicon wafer thinning

Glass Wafers

Silicon wafers are very common in wafer fabrication facilities. A silicon carrier wafer is a very close match to the device substrate wafer. A silicon carrier wafer can be a lower grade wafer and does not have the device specific layers. Thus it may be a good choice as a carrier wafer in development activities. However, as the thinning process for 3D-IC transfers into production it is illustrative to consider other alternatives.

Corning has been providing glass solutions for a variety of industrial and consumer applications for more than 160 years. Among recent applications enabled by Corning's precision flat glass process technology is the liquid crystal display (LCD) substrate. This platform is an attractive option for development to supply alternative high volume substrate material as a new kind of glass wafer carrier for the semiconductor industry.

Glass carrier wafers have some unique advantages over silicon carrier wafers. Since the glass wafer is transparent, it is much easier to observe any bonding defects that may occur during process development. In addition, some of the temporary bonding polymers require a transparent substrate for explicit optical processing steps for bonding or debonding that are enabled by transparent glass carriers. The optical transmission spectrum of Corning glass wafers is shown in figure 2.

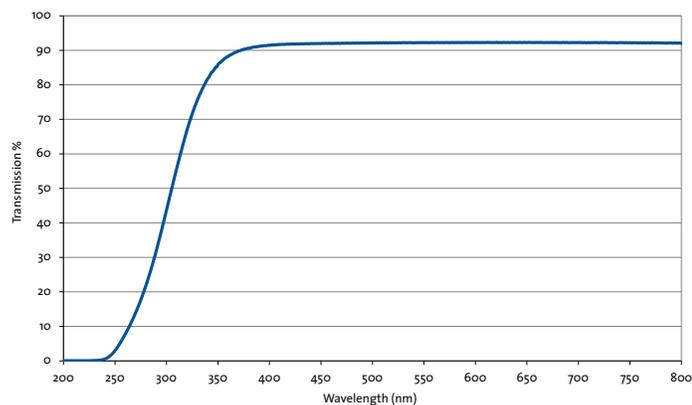


Figure 2. Glass Wafer Transmission

Physical Dimensions

The history of Corning glass for LCD displays was recently published highlighting the fusion process for making glass [1, 2]. In this process the glass flows over the edges on both sides of a trough rejoining underneath the trough. The fusion process is shown in figure 3. The pristine outer edges of the glass do not touch any of the forming surfaces and are contact free. As a result, the surface of the glass is extremely smooth and defect free, as shown by the atomic force microscopy images in figure 4.



Figure 3. The Corning Fusion Process

The fusion process is capable of providing precision glass sheet with dimensions over 3 meters. A critical feature of the fusion process for LCDs is to minimize thermal stress effects in the glass. Any area of thermal stress will result in birefringence that could cause visible artifacts. This is a very good feature for glass carriers created from fusion glass. With very little thermal stress in the glass carrier, the warp can be very low. The wafer shown in figure 5 has a maximum warp of only 12 μm . It was measured on a National Institute of Standards traceable, Corning Tropel Flat Master MSP 300.

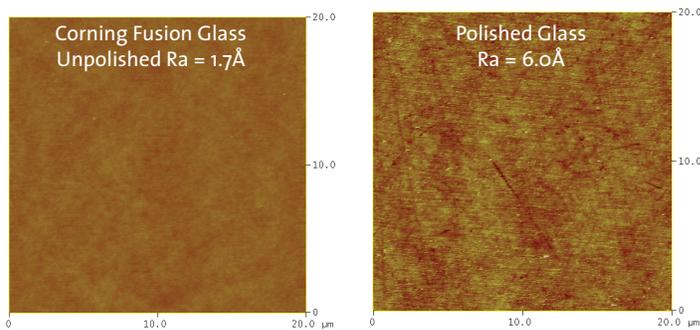


Figure 4. Atomic force micrograph result

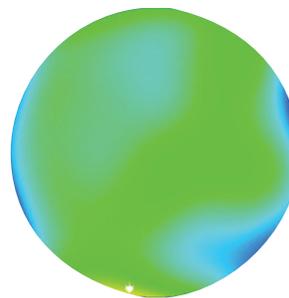


Figure 5. Glass wafer with maximum warp of 12 μm

The glass wafers are cut from special fusion sheets to meet the needs of a silicon carrier wafer. Generally the glass wafers follow all the requirements of the semiconductor silicon wafer M1 standard [3]. For example, the glass wafers have the same edge bevel and notch as any standard silicon wafer. Figure 6 shows an example of the edge bevel and notch on a glass wafer. Because they come from a sheet the final diameter of the carrier can be arbitrarily specified up to 450 mm in diameter. This means that it is straightforward to specify a 201 mm glass wafer as a carrier for a 200 mm Si wafer, for example. In addition, the glass wafers can also incorporate the standardized T7 or QR labeling code requirements on the backside surface or even embedded within the bulk volume.

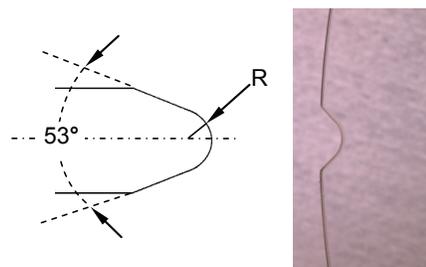


Figure 6. Glass edge and notch example

When using the temporary bond/debond process for thinning operations, it is important that the carrier/adhesive/wafer stack has a total thickness variation (TTV) that is minimized and less than a few microns. This means that the carrier wafer must start out with very low TTV. The other important point about using the fusion draw process is that it can be leveraged to produce wafers with exceptionally low total thickness variation (TTV). Figure 7 shows a glass wafer with TTV less than 2 μm with no polishing. Because no polishing is required it allows for easier volume scaling.

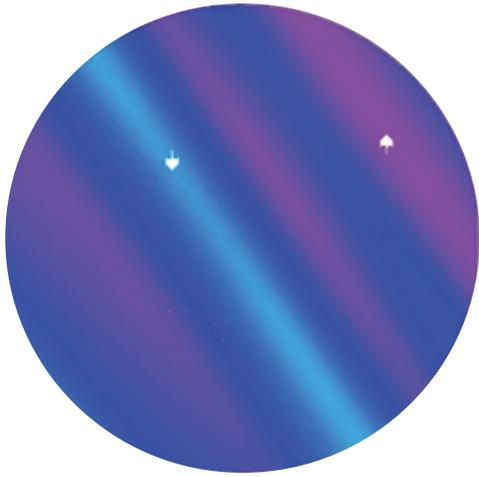


Figure 7. Glass wafer with TTV less than 2 μm

Mechanical Parameters

Table 1 lists the mechanical properties of silicon wafers compared to Corning glass wafers. It can be seen the thermal expansion coefficient of the Corning glass wafers is nearly identical to silicon wafers in the temperature ranges normally encountered in packaging process operations. This is an important parameter depending on the thermal profiles encountered in the backend processes.

Mechanical Properties	Corning Glass	Silicon
Density (g/cm ³)	2.38	2.33
Young's Modulus (GPa)	73.6	129.5 [100]
Knoop Hardness (kg/mms)	453	1150
CTE (0-300°C, x10 ⁻⁷ /°C)	31.7	31.5

Table 1. Glass and Silicon Mechanical Properties

Strength Parameters

Wafer breakage is a major concern in semiconductor manufacturing lines since it results in significant costs and disruptions. Silicon wafers typically break by cleaving along crystallographic planes. Glass breaks by brittle fracture. However, both substrates are considered highly brittle materials. This means for both materials their strength depends on the presence of flaws (micro-cracks, etch pits, etc.) rather than the intrinsic material properties. When more flaws exist, there is a higher statistical probability of failure when loads/stresses are applied to the wafer during manufacturing processes. This increases the importance of methods used in wafer preparation, making management of grinding and polishing processes extremely important. [4] In the next sections, we discuss some baseline data on the practical strength of glass and silicon surfaces and edges.

Even though the fracture modes are different it is useful to compare the fracture strength of a silicon wafer surface to a glass wafer surface by using standardized test methods. A ring-on-ring test is appropriate for surfaces or a three point bend test can be used for edges (see figure. 8). The ring-on-ring technique consists of two concentric rings. The larger ring is positioned on the bottom, the smaller ring on top and the wafer under test placed between the two rings. The force is applied to the top ring creating a region of uniform tensile strain in the lower surface of a wafer material. The applied force is increased until failure occurs by fracture from a flaw.

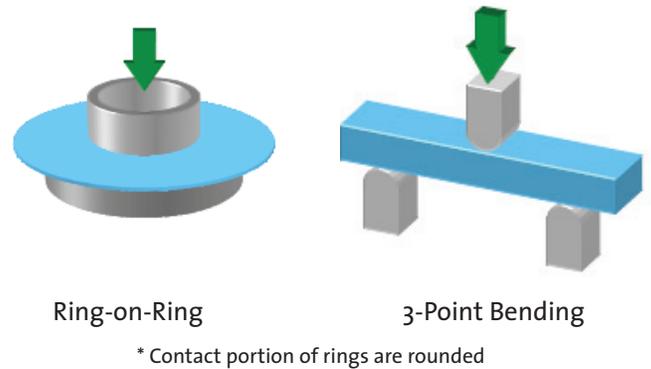


Figure 8. Schematic of a ring-on-ring test and 3-point bending to evaluate failure stress at a surface or an edge.

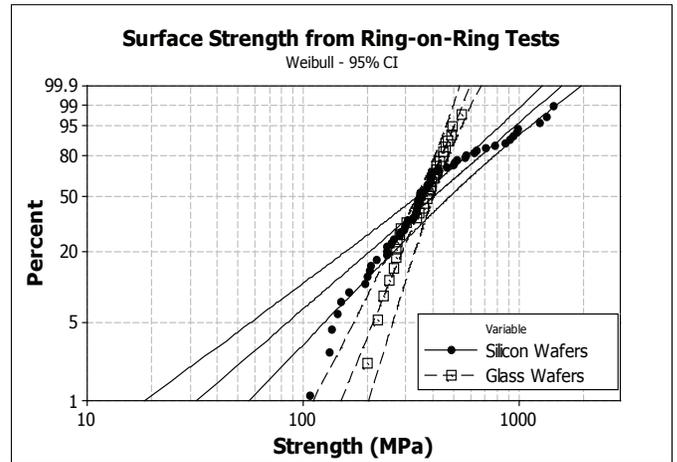


Figure 9. Weibull plot of silicon and glass wafer fracture loads

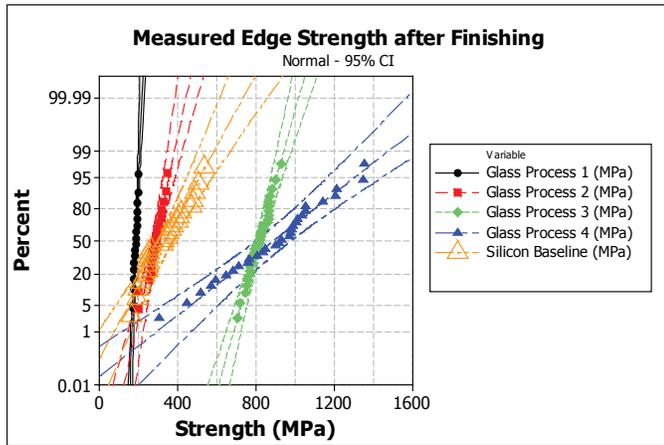


Figure 10. Weibull plot of silicon and glass wafer edge fracture loads

A significant advantage of Corning’s fusion process is that it provides an extremely high quality, precision surface that exhibits high strength without any processing. This avoids potentially strength limiting flaws that can be left behind by grinding/polishing. To evaluate the statistical nature of the failures it is useful to put the fracture data onto a Weibull plot. Figure 9 shows a Weibull distribution of 300 mm diameter silicon wafers (0.785 mm thick) and glass wafers (0.5 mm thick). The median strength values are almost identical for both materials. The relatively steep slope given by the glass wafers in Fig. 9 results in a more repeatable, predictable performance and avoids the very low strength specimens seen in the silicon population.

A high percentage of wafer failures occur at the ground edge of Si wafers. [4] This makes the wafer edge strength a very important attribute and strongly dependant on the edge finishing methods. Figure 10 shows Weibull distributions of the edge strength of several types of wafers measured by horizontal 3-point bend tests. The open triangles show data from standard silicon wafers. The other four data sets give the strength distribution for glass wafers prepared by four different finishing processes. Process 1 had relatively low edge strength relative to silicon and Process 2 had a mean strength close to that of silicon. However, Processes 3 and 4 provided edge strength that is substantially higher than that of silicon. The relatively low slope of Process 4 indicates that additional development is required to improve the reliability of the strength, but the high end strength is attractive.

The data in Fig. 10 demonstrates that it is not the material (glass vs. silicon) that dictates the edge strength, and therefore the reliability of the wafer, but it is how well the material is processed during wafer preparation. From a mechanical strength perspective, Corning fusion glass is very well suited to be used in these applications.

Conclusions

Glass wafers derived from extensions of Corning’s fusion process have many attributes that make them attractive for use as carrier wafers in semiconductor manufacturing processes. Fusion is a mature manufacturing process that produces extremely high quality glass wafers with very low TTV and low warp. The wafers are cut from sheets, which makes it straightforward to scale up to 450 mm diameter wafers. Corning’s glass wafers have a CTE that closely matches that of silicon wafers, which is advantageous in avoiding deformation as the wafer stacks are heated and cooled. The optical properties of the material allow for easy inspection techniques to evaluate the quality of the bonds as well as other light/laser based processing. Since glass is a brittle material like silicon, it is important to carefully manage finishing processes. The glass is formed in thin sheets to a target thickness in the fusion process. Therefore it is not necessary to grind and polish the surface, thus avoiding strength limiting micro-flaws that can remain on the surface. Finally, it was shown that glass edges can be extremely strong when processed correctly. We have shown properties of Corning glass wafers to similar properties of silicon wafers.

References

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